IN THE CLAIMS

1-24. (Canceled)

25. (Currently Amended) A Method of improving immunity to interference of an integrated circuit ~~(16)~~, the method comprising:
sending a pair of logically complementary error signals from respective first and second independent processor cores to at least one further component ~~(2)~~; and
evaluating the error signals in the at least one further component when each of the error signals has maintained its respective logic state for at least a minimum pulse length.

26. (Previously Presented) A method according to claim 25, wherein the further component is a mixed-signal module.

27. (Previously Presented) A method according to claim 25, wherein in the event of a sequence of pulses on at least one of the error signals with a distance between the pulses that is smaller than the minimum pulse length, the time of the sequence of pulses output over a respective one of the error signals is extended with respect to the actual pulse sequence time.

28. (Previously Presented) A method according to claim 25 further comprising filtering the error signals.

29. (Currently Amended) A method according to claim 25, wherein at least one watchdog time window ~~(17)~~ is predetermined in the at least one microprocessor chip or multiple processor µC ~~(1)~~ or in the further component ~~(2)~~, within which at least one test pulse is generated on the error signals.

30. (Currently Amended) A method according to claim 29, wherein the watchdog time window ~~(17)~~ has a delay time TWindowDelay, and the time window, in which at least one error signal or error signal pattern is expected, remains open until the expiry of the delay time TWindowDelay.

31. (Currently Amended) A method according to claim 30, wherein the delay time TWindowDelay is longer than ~~the~~ a filter time TFilter of filters ~~(7, 7')~~ processing the error signals.

32. (Currently Amended) A method according to claim 30, wherein the time window TWindowDelay is set in the further component ~~(2)~~ by way of an interface ~~(5)~~ connected to at least one microprocessor chip or multiple processor µC ~~(1)~~.

33. (Previously Presented) A method according to claim 30, wherein a condition TWindowDelay is satisfied in excess of the filter time TFilter.

34. (Previously Presented) A method according to claim 30, wherein the delay TWindowDelay approximately corresponds to twice the time TFilter.

35. (Previously Presented) A method according to claim 25 further comprising extending durations of pulses on the error signals.

36. (Currently Amended) A method according to claim 25, wherein a test of the error signals ~~(3, 4)~~ is performed with the aid of an interface ~~(5)~~.

37. (Currently Amended) A method according to claim 25, wherein the error signals are filtered by filters ~~(7, 7')~~ with a defined filter time TFilter.

38. (Previously Presented) A method according to claim 25, wherein the pulse width TMin is set to a value of at least 30 nanoseconds approximately.

39. (Currently Amended) An integrated circuit comprising:

at ~~least one microprocessor chip or multiple processor microcontroller (1) or microprocessor module~~least a first and second independent processor core;
at least one additional separate component ~~(2)~~ having separately arranged power elements; and
one or more pulse extending devices or signal delaying devices for outputting error pulses ~~(6, 6')~~ one after another through a logically complementary pair of error lines ~~(3, 4)~~.

40. (Currently Amended) An integrated circuit according to claim 39 further comprising: one or more filters ~~(7, 7')~~ for filtering the error pulses transferred through the error lines ~~(3, 4)~~.

41. (Currently Amended) An integrated circuit comprising:

at least ~~one microprocessor chip or multiple processor microcontroller (1)~~a first and second independent processor core;

at least one additional component ~~(2)~~ having separately arranged power elements, wherein a complementary pair of error signals transferred between the at least one ~~microprocessor chip or multiple processor µC (1)~~first and second independent processor core and the at least one additional component ~~(2)~~; and

filters ~~(7, 7')~~ for filtering error pulses ~~(6, 6')~~ through associated ones of the error signals ~~(3, 4)~~.

42. (Currently Amended) An integrated circuit according to claim 41, wherein each filter ~~(7, 7')~~ is configured as a digital forward/backward counter.

43. (Currently Amended) An integrated circuit according to claim 41, wherein the chips or components are interconnected by at least one bus ~~(5)~~ and at least one error line ~~(3, 4)~~.

44. (Currently Amended) An integrated circuit according to claim 43, wherein the circuit includes hardware test structures, with the aid of which a test of the at least one error line ~~(3, 4)~~ can be performed using an interface ~~(5)~~.

45. (Currently Amended) An integrated circuit according to claim 41, wherein the ~~microprocessor chip (1)~~first and second independent processor core or the additional component comprises at least one watchdog window circuit ~~(50)~~.

46. (Currently Amended) An integrated circuit according to claim 45, wherein the watchdog window circuit ~~(50)~~ predefines a watchdog time window ~~(17)~~, and the watchdog time window ~~(17)~~ has a delay time TWindowDelay, and the time window, in which at least one error signal or error signal pattern is expected, remains open until the expiry of the delay time TWindowDelay.

47. (Currently Amended) An integrated circuit according to claim 45, wherein the delay time TWindowDelay is longer than the filter time TFilter of the filter(s) ~~(7, 7')~~ processing the error signal(s) of the at least one error line ~~(3, 3')~~.